forming a first contact layer composed of GaAs or InGaAs doped with n type impurities, on the electric field strength reducing layer;

forming a recess stopper layer composed of intrinsic InGaP, on the first contact layer;

forming, on the recess stopper layer, a second contact layer composed of GaAs doped with n type impurities of a concentration higher than that of the first contact layer;

wet-etching the second contact layer to form a wide recess opening penetrating the second contact layer using the recess stopper layer as a stopper;

forming a source electrode and a drain electrode on the second contact layer outside the wide recess opening so that the wide recess opening is sandwiched between the source electrode and the drain electrode;

wet-etching the first contact layer in the wide recess opening using the electric field strength reducing layer as a stopper;

wet-etching the electric field strength reducing layer in the wide recess opening to form a narrow recess opening penetrating the recess stopper layer, the first contact layer, and the electric field strength reducing layer using the first electron supply layer as a stopper; and

forming a gate electrode on a surface of the first electron supply layer exposed from a bottom of the narrow recess opening.

14. The manufacturing method for a heterojunction type compound semiconductor field effect transistor according to claim 13, wherein the compound semiconductor substrate includes a semi-insulating GaAs substrate, a buffer layer deposited and formed on the semi-insulating GaAs substrate and having a superlattice structure, and a second electron supply layer deposited and formed on the buffer layer and under the channel layer and composed of AlGaAs doped with n type impurities.

15. A manufacturing method for a heterojunction type compound semiconductor field effect transistor, the method comprising:

forming a channel layer composed of intrinsic GaAs or InGaAs on a compound semiconductor substrate;

forming a first electron supply layer composed of AlGaAs on the channel layer;

forming an electric field strength reducing layer composed of intrinsic InGaP on the electron supply layer;

forming a first contact layer composed of GaAs or InGaAs doped with n type impurities, on the electric field strength reducing layer;

forming a recess stopper layer composed of intrinsic InGaP, on the first contact layer;

forming, on the recess stopper layer, a second contact layer composed of GaAs doped with n type impurities of a concentration higher than that of the first contact layer;

wet-etching the second contact layer using the recess stopper layer as a stopper;

wet-etching the recess stopper layer to form a wide recess opening penetrating the second contact layer and the recess stopper layer using the first contact layer as a stopper;

forming a source electrode and a drain electrode on the second contact layer outside the wide recess opening so that the wide recess opening is sandwiched between the source electrode and the drain electrode;

wet-etching the first contact layer in the wide recess opening using the electric field strength reducing layer as a stopper;

wet-etching the electric field strength reducing layer in the wide recess opening to form a narrow recess opening penetrating the first contact layer and the electric field strength reducing layer using the first electron supply layer as a stopper; and

forming a gate electrode on a surface of the electron supply layer exposed from a bottom of the narrow recess opening.

16. The manufacturing method for a heterojunction type compound semiconductor field effect transistor according to claim 15, wherein the compound semiconductor substrate includes a semi-insulating GaAs substrate, a buffer layer deposited and formed on the semi-insulating GaAs substrate and having a superlattice structure, and a second electron supply layer deposited and formed on the buffer layer and under the channel layer and composed of AlGaAs doped with n type impurities.

17. A manufacturing method for a heterojunction type compound semiconductor field effect transistor, the method comprising:

forming a channel layer composed of intrinsic GaAs or InGaAs on a compound semiconductor substrate;

forming a electron supply layer composed of AlGaAs on the channel layer;

forming an electric field strength reducing layer composed of intrinsic InGaP on the first electron supply layer;

forming a first contact layer composed of GaAs or InGaAs doped with n type impurities, on the electric field strength reducing layer;

forming a recess stopper layer composed of intrinsic InGaP, on the first contact layer;

forming, on the recess stopper layer, a second contact layer composed of GaAs doped with n type impurities of a concentration higher than that of the first contact layer;

wet-etching the second contact layer to form a wide recess opening penetrating the second contact layer using the recess stopper layer as a stopper;

forming a source electrode and a drain electrode on the second contact layer outside the wide recess opening so that the wide recess opening is sandwiched between the source electrode and the drain electrode;

wet-etching the recess stopper layer in the wide recess opening using the first contact layer as a stopper;